COMPARATIVE STUDY OF THE TOPOLOGIES OF MULTILEVEL INVERTER

Himadri Ghildiyal*

Himani Pande*

Prateek Gupta*

ABSTRACT

The multilevel inverter topologies have proved recently as very important alternative in the area of high power and medium voltage energy control .This paper presents the comparison of different topologies of multilevel inverter that are diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel inverter. The paper also presents the comparison of the topologies in terms of total harmonic distortion. The main function of multilevel inverter is to obtain a desired ac voltage from several levels of dc voltages. As we increase the number of voltage levels, the harmonic content decreases significantly. These multilevel inverters are used to increase inverter operating voltage, to minimize THD with low switching frequency, to reduce EMI due to lower voltage steps. The advantages of this multilevel approach includes good power quality, good electromagnetic compatibility, low switching losses and high capability. This project proposes to study various multilevel topologies, to compare the topologies and the levels. The main objective of this study is to reduce total harmonic distortion, comparison of THD and fundamental component for different modulating techniques.

***Keywords**: Multilevel Inverter, DCMLI, FCMLI, CHBMLI, THD.*

*Department Of Electrical Engineering, College Of Engineering Roorkee, Roorkee, India

I. INTRODUCTION

Various industrial applications require higher power apparatus. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is very difficult to connect only one power semiconductor switch directly to it. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables an efficient use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily connected to a multilevel converter system for a high power application.

The concept of multilevel inverters has been introduced since 1975. The functioning of multilevel inverter began with three level converter. Several advancements have been made tiil date that includes development of various topologies that are very efficiently used these days in the industrial field. The basic concept of a multilevel inverter to achieve higher power is to use a series of power semiconductor switches with several low voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform that is ac in nature. Capacitors, batteries, and other renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

II. MULTILEVEL PRINCIPLE

The multi-level inverter [1-3] includes an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. This paragraph has the aim to introduce to the general principle of multilevel behavior. The general idea of multilevel converters is to synthesize a sinusoidal voltage from several voltage-levels, typically obtained from capacitor voltage sources. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion.

III. Multilevel Inverter Topologies

A. Diode Clamped Multilevel Inverter:

The most commonly used multilevel topology is the diode clamped inverter in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. The voltage across each capacitor for an N level diode clamped inverter [4-5] at steady state is $V_{dc}/(n-1)$. Although each active switching device is only required to block $V_{dc}/ n-1$, the clamping devices have different ratings. The diode clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. Fig. 1 shows a three phase three level diode clamped multilevel inverter.

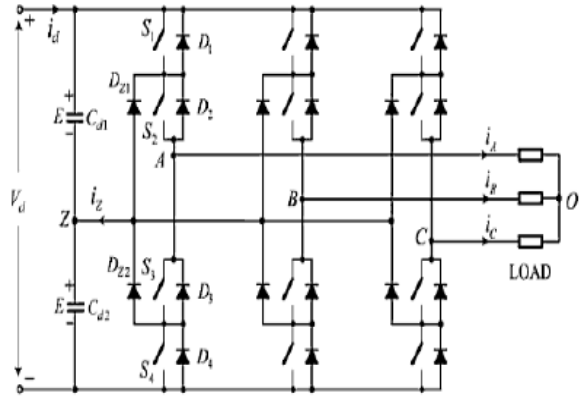

Fig.1 Three phase three level diode clamped multilevel inverter

An m level inverter leg requires 2(m-1) switching devices and (m-1)(m-2) clamping diodes. For a three level inverter, m=3, so it needs 4 switching devices and 2 clamping diodes per leg as shown in fig. (1).

(1) For an output voltage of Va = Vdc, all the upper half switches of a- phase leg are turned ON i.e S1 and S2 are ON.

(2) For output voltage of Va = Vdc/2, only S2 and S3 are ON.

(3) For output voltage of Va = 0, the lower half switches of a- phase leg are turned ON i.e. S3 and S4 are ON.

Table 1 shows the voltage levels and their corresponding switch states. State condition 1 means the switch is ON and state condition 0 means the switch is OFF. It should be noticed that there are two complementary switch pairs. These pairs for one leg of the inverter are (S1, S3) and (S2, S4).

Table 1 Switch states for various voltages of a phase leg.

Voltage level V_a=	S_{A1}	S_{A2}	S_{A3}	S_{A4}
V_{dc}	1	1	0	0
$V_{dc}/2$	0	1	1	0
zero	0	0	1	1

Thus, if one of the complementary switch pairs is turned ON, the other of the same pair must be OFF. Two switches are always turned ON at the same time. Output voltage waveform of a three level diode clamped inverter is as shown in fig. 2.

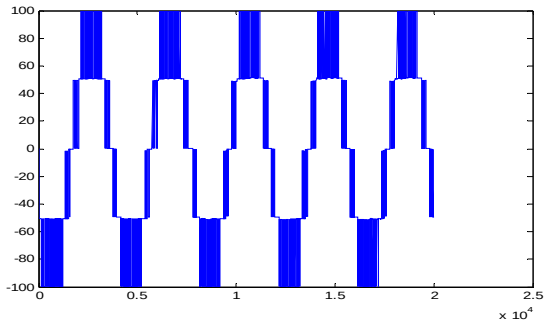

Fig. 2 Output voltage of three level Diode Clamped Multilevel Inverter.

B. Flying Capacitor Multilevel Inverter:

The flying capacitor muitilevel inverter [6] is relatively new compared to diode clamped and cascaded h bridge multilevel inverter. Figure 2.2(a) shows one phase of a three phase three level flying capacitor multilevel inverter. In this topology each capacitor is charged to a different voltage level and by changing the transistor switching states, the capacitors and dc source are connected in different ways and produce various line to ground output voltages. For the analysis presented herein the line - to- ground voltage and capacitor currents are of interest. From the topology KVL and KCL equations, these quantities can be expressed as:

$$V_{ag}=(T_{a3})V_{dc}+(T_{a2}-T_{a3})V_{c2a}+(T_{a1}-T_{a2})V_{c1a}$$

$$i_{c1a}=(T_{a2}-T_{a1})\,i_{as}$$

$$i_{c2a}=(T_{a3}-T_{a2})\,i_{as}$$

Based on these fundamental equations, the line - to – ground voltage and capacitor currents, can be determined for all combinations of transistor signals as shown in table 2.

The three phase implementation involves three branches of the structure shown in fig 3 connected in parallel on the dc side and connected to a wye configured load on the ac side.

Table 2 Three level FCMI output voltages

T_{a1}	T_{a2}	T_{a3}	v_{ag}	i_{c1a}	i_{c2a}
0	0	0	0	0	0
0	0	1	$v_{dc}-v_{c2a}$	0	i_{as}
0	1	0	$v_{c2a}-v_{c1a}$	i_{as}	$-i_{as}$
0	1	1	$v_{dc}-v_{c1a}$	i_{as}	0
1	0	0	v_{c1a}	$-i_{as}$	0
1	0	1	$v_{dc}-v_{c2a}+v_{c1a}$	$-i_{as}$	i_{as}
1	1	0	v_{c2a}	0	$-i_{as}$
1	1	1	v_{dc}	0	0

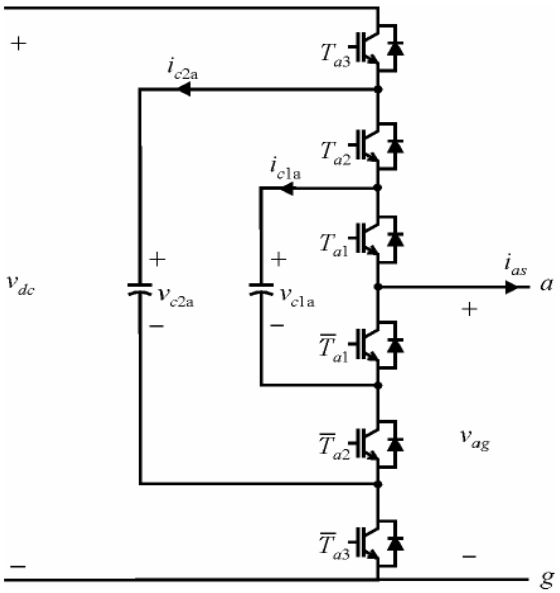

Fig. 3 The three level FCMI inverter topology (a- phase)

The output of a three phase three level flying capacitor multilevel inverter is as shown in fig. 4

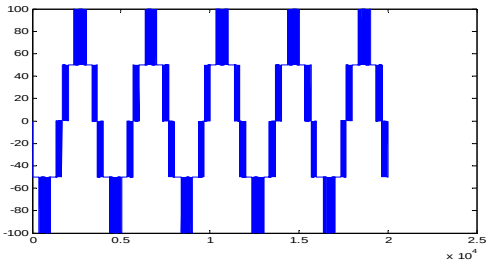

Fig. 4 Output voltage waveform of three level flying capacitor multilevel inverter

C. Cascaded H Bridge Multilevel Inverter

In cascaded H bridge [7-9] topology the H- bridges are cascaded in every phase. With the increase in H-bridges in a phase, the output voltage waveform tends to be more sinusoidal. Fig. 5 shows its 3- level topology. It consists of 2 identical H-bridges in each phase. In n level topology , (n-1)/2 identical H-bridges are used in each phase. There must be a separate DC source for the DC bus of every individual H-bridge. Hence this topology is useful for collecting energy from renewable energy resources eg. solar panels and fuel cell.

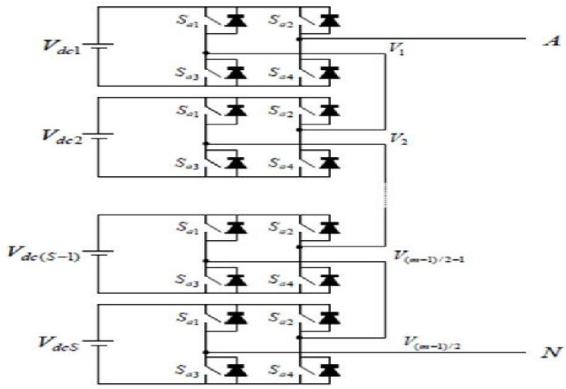

Fig. 5 Three level cascaded H bridge Multilevel Inverter

A cascaded multilevel inverter is made up from series connected single full bridge inverter each with their own isolated DC bus. This multilevel inverter can generate almost sinusoidal waveform voltage from several separate dc sources, which may be obtained from solar cells, fuel cells, batteries ultra capacitors etc. This type of converter does not need any transformers, or clamping diodes or flying capacitors. Each level can generate five different voltage outputs +2Vdc, +Vdc, 0, -Vdc, -2Vdc. by connecting the DC sources to the AC output side by different

combinations of the four switches. The output voltage waveform of an M- level inverter is the sum of all individual inverter outputs.

IV. COMPARISION OF TOPOLOGIES IN TERMS OF THD

The THD [10-12] for diode clamped multilevel inverter is as shown in fig. 6. The optimal value of modulation index of 0.8 and switching frequency of 750 hz has been selected to get much better performance. The THD is decreased significantly to 17.53%. Also it is observed that 7th harmonic is reduced significantly.

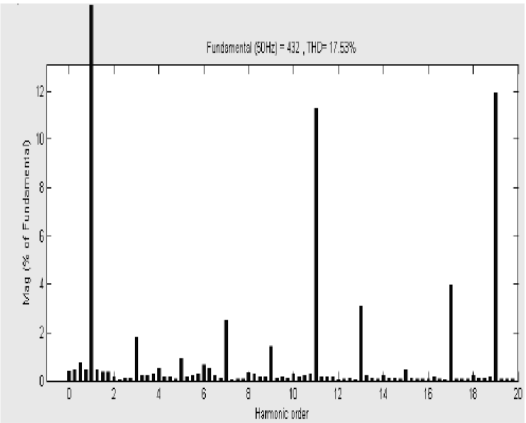

Fig. 6 Harmonic Spectrum of DCMLI

Fig. 7 shows the harmonic spectrum for the output phase voltage of a three level flying capacitor mli. It is shown that 26.35% of harmonics present in the line- line voltage i.e. the THD will decrease significantly to 26.35%. Switching frequency of 500 Hz and flying capacitors of 3344µF has been selected for this topology.

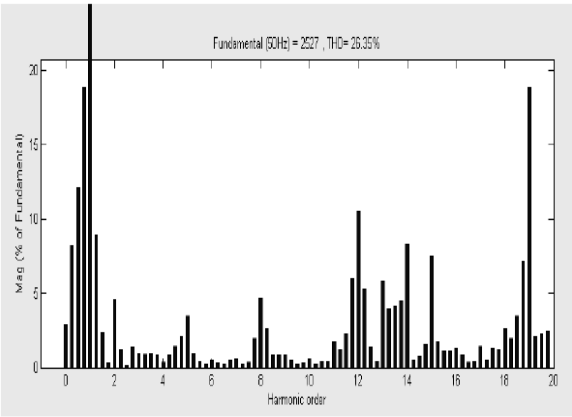

Fig. 7 Harmonic spectrum of FCMLI

Simulation of cascaded H bridge inverter yields harmonic spectrum as shown in fig. 8. The THD is significantly reduced to 12.01%. Also the most of the lower order harmonics are suppressed.

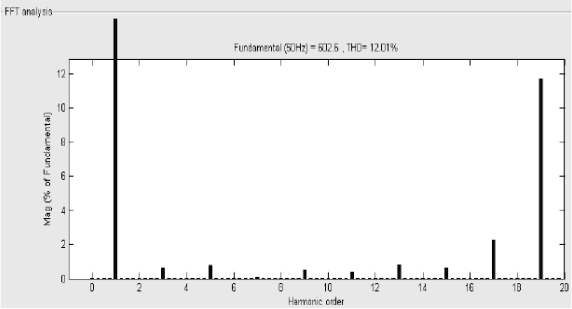

Fig. 8 Harmonic Spectrum of CHB Inverter

V. COMPARISIONS

Table 3 : Comparision of THD

Power circuit topology	V line- line THD (%)
3 level FCMLI	26.35
3 level DCMLI	17.53
3 level CHBMLI	12.01

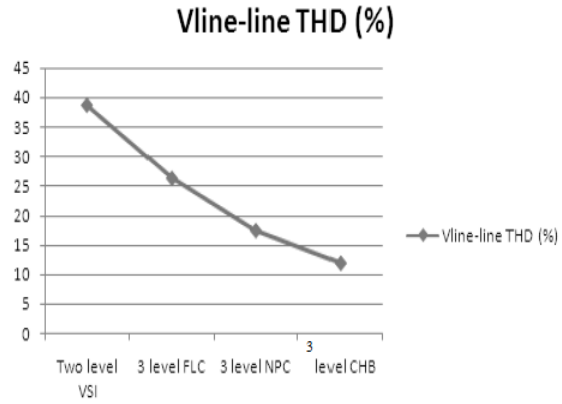

Fig 9 Comparision of THD for all the investigated topologies.

VI. RESULT

The topologies have been compared in terms of structure , cost and efficiency. The voltage waveforms of the three level inverters show that the voltage across the motor contains not only the “fundamental” sinusoidal component but also pulses of voltage i.e. the harmonics are high. In case of DCMLI, main drawbacks are the requirement of clamping diodes, lack of modularity and

unequal semiconductor loss distribution. The additional expense of FC, particularly at low carrier frequency and a high number of cells are main disadvantage of FC topology. For CHB, main disadvantage is the separate DC sources usually provided by a bulky and non- standard transformer. CHB is particularly necessary for very high power applications.

VII. CONCLUSION

This paper proposes the three multilevel topologies (3L DCMLI, 3L FCMLI and 3L CHBMLI) and they cover different needs for different types of applications. The harmonic spectrum of the three topologies are studied and it is shown by FFT analysis that the output voltage includes THD along with the fundamental voltage. It is seen that 3 L CHB has minimum THD content and 3L FCMLI has maximum THD content. It was shown that the output voltage levels are increased in the multilevel inverter to approach near sine wave and to get the higher voltage and reduced THD.

VIII. References

[1] J.S. Lai and F.Z. Peng,*"Multilevel Converters- A new breed of power converters"*, IEEE Trans. Ind.Applicat., vol. 32, pp. 509-517, May/June 1996

[2] L.Tolbert, F.Z.Peng, T.Habetler, *"Multilevel converter for large electrical drives"*, IEEE Trans.Ind.Applicat., vol. 35, pp. 36-44, Jan/Feb. 1999

[3] R.Teodorescn, F.Beaabjerg, J.K.Pederson, E.Cergelei, S.Sulistijo, B.Woo, and P.Enjeti, *"Multilevel converters- a survey"*, in Proc. European Power Electronics Conf (EPE '99), Lansane, Switzerland, 1999

[4] V.Naga Haskar Reddy, Ch.Sai.Babu and K.Suresh- *"Advanced Modulating Techniques for diode clamped multilevel inverter"*, ISSN 1819-6608, vol.6 no.1 Jan. 2011

[5] Sule Ozdemir, Engin Ozdemir, Leon M.Tolbert and Surin Khomfoi, *"Elimination of Harmonics in a five level diode clamped multilevel inverter using fundamental mod."*, PEDS 2007

[6] Y.Liang, C.O. Nurankpa, *" A powerline conditioner based on flying capacitor multilevel voltage source inverter with phase shift SPWM"*, IEEE transactions on industry applications, vol. 36, no. 4, pages 965-971, July 2000

[7] M.Kavitha, A.Arunkumar, N.Gokulnath, S.Arun, *"New cascaded H bridge Multilevel Inverter topology with reduced no. of switches and sources"*, ISSN: 2278-1676, vol- 2 issue- 6 (sep-oct 2012), pp 26-36

[8] P.Palanivel and Subhransu Sekhar Dash, *"Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier PWm Techniques"*, IET Power Electronics. Vol. 4 issue 8, Sep 2011, pp 951- 958

[9] P.Palanivel and Subhransu Sekhar Dash, *"Comparative study of constant switching frequency and variable switching frequency multicarrier PWM for 3 phase multilevel inverter"*, International Journal of recent trends in Engg, Vol 2, no. 7, Nov. 2001, pp 49-52.

[10] M.Ghasem Hosseini Aghdam, S.hamid Fathi, Gevorg B.Gharehpetian, (2008) *"Harmonic optimization techniques in multilevel vsi with unequal DC sources"*, Journal of Power Electronics, Vol. 8, no. 2

[11] Zhong Du, Burak Ozpineci and Leon M.Tolbert, (2007) *"Modulation Extension Control of hybrid Cascaded H- Bridge multilevel conv. with 7 level fundamental frequency switching scheme"*, IEEE 2007

[12] T.Prathiba, P.Remga, *"A comparative study of total harmonic distortion in multilevel inverter topologies"*, Journal of information Engg and applications ISSN 2224- 5782 (print) ISSN 2225- 0506 (online) vol. 2 no. 3, 2012