CLOCK GATED LOW POWER 64-BIT REGISTER DESIGN

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ABSTRACT

We achieve 25% power reduction in clock gated 64-bit Register design when we provide clock period of 2 ns to 64-bit register. We again achieve 16.66% power reduction in 64-bit Register when we provide clock period of 2 ns to 64-bit register. Clock gating reduces dynamic power dissipation in 64-bit register but increases junction temperature of device. Xilinx planahead 14.1 is used as simulator and Virtex-6 is used as 40-nm FPGA device for implementation purpose. We apply clock gate to inhibit clock when device is not in use, in order to reduce power dissipation.

Keywords*—Sequential Circuit, Low Power, Clock Gating, Glich Free Design, Register Transfer Level, Register, LUT, Buffer.*

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I. INTRODUCTION

Dynamic power consists of clock power along with signal power, IOs power and logic power. Only Clock power contributes 45-60 percent of total dynamic power. Hence, reducing clock power is very important. In order to reduce clock power dissipation, we design a small circuit called clock gate. Clock gate is a logic gate which takes clock in form of input and produce gated clock in form of output.

$$ClockGate = Clock + Gate(either\ AND\ or\ OR)$$

It has 2 instances and 3 nets. When ctr is logic low then it prohibit supply of clock and gated off the device and reduce power dissipation too.

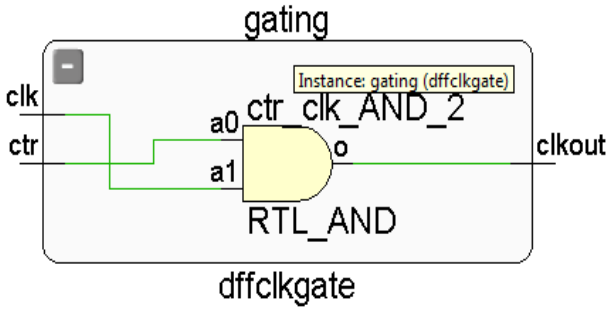

Figure 1: Schematic of Clock Gate

Clock Gated 64-bit Register contains 3 Instances, 131 input or output ports and 135 nets. A net is a set of interconnected pins and wires. Every wire has a net name, which identifies it to the Schematic and Symbol Editors and netlister programs. Two or more wires can have the same net name. In a net, all wire share the same name and all symbol pins connected to these wires are electrically connected. Buses are a convenient way to group related signals. However, buses can be any group of signals, related or not.

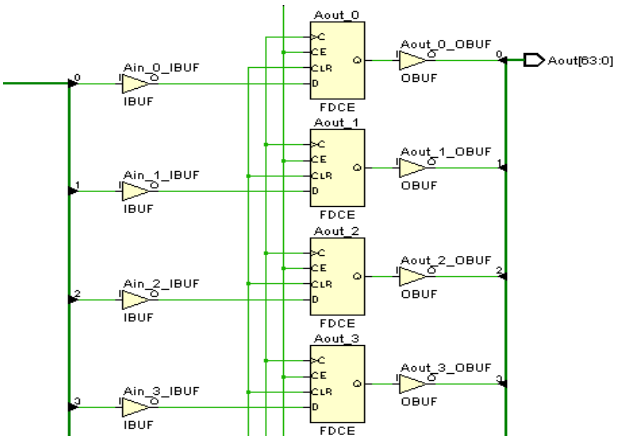

Figure 2: Schematic of 64-bit Register Aout_0-Aout_63

This Register has 64 D flip-flop. First D flip-flop is Aout_0 and last flip-flop is Aout_63. Aout_0 has one input buffer called Ain_0. Aout_0 has one output buffer called Aout_0.

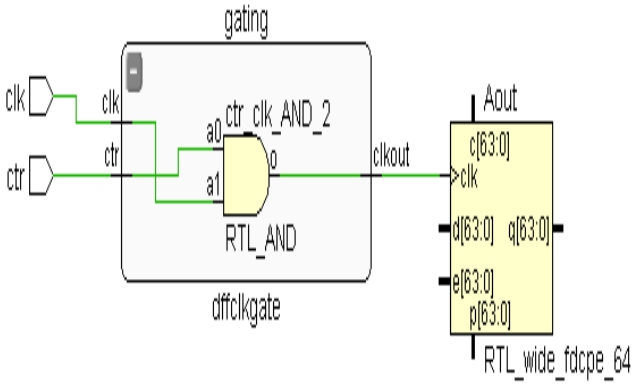

Figure 3: Application of Clock Gate to 64-bit Register

We apply clock gate to 64-bit register in order to reduce dynamic power consumption of register. If ctr is 0 then clk will not reach to register and register will switched off. When register is in off state, it will not consume power. In that way, we achieve our goal of power saving. Area is a trade-off in this technique. Using Clock gating, we decreases clock power, signal power but increases IO power and ineffective in case of leakage power.

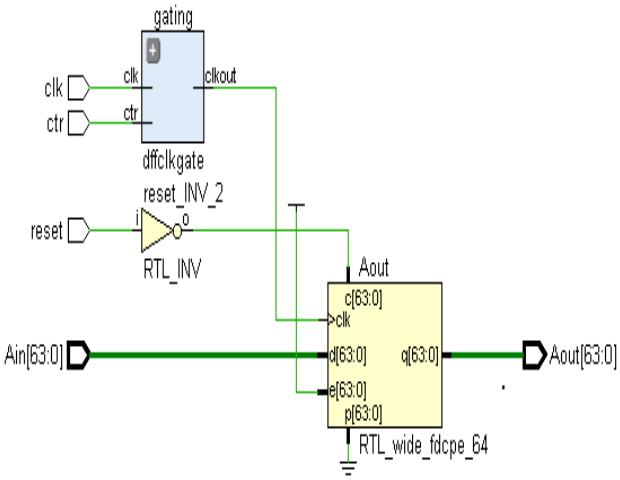

Figure 4: Clock Gated Low Power 64-Bit Register Design

II. RELATED WORK

In reference [1], clock gating techniques such as Valid Clock Gating, Idle State Based Clock Gating and Observability don't care based Clock Gating are three techniques to achieve reduction in power consumption. Idle state based clock gating is taken into consideration when the current state value and the next state value of an FF are the same, it is unnecessary for the FF to transmit the next state value in the next clock cycle. Therefore, it is valid to freeze the

FF under such situation. Observability don't cares (ODC) of a Boolean variable are the conditions under which the variable is not affecting any of the primary outputs (PO). If the next state value cannot be observed in the coming clock cycles, the FF can be clock gated in those clock cycles. Works in [1], extended the theory of determining valid clock gating conditions to cover originally invalid conditions for more power savings. And [1] also introduced a procedure of finding error cancellation based clock gating conditions. In paper [2], Latch-free based design; Latch-based design and Flip-flop based design are many clock gating styles available to optimize power in VLSI circuits. According to [2], paper raise issues in implementation of clock gating design techniques. The clock gate (i.e., AND or OR) must not alter the waveform of the clock other than switching the clock on or off is first issue. Clock gating holds time violations and set-up time violations can be fixed like other violations during physical design phase is other issue in clock gating. Reference [2] proposes some techniques which can used to fix hold violations are clock skewing/buffering in data path near to endpoint. The main motive of [2] deals with Glitches-transient fault, which occur due to design error. Techniques in [3], achieved 93.75% clock power reduction in ALU. Reduction of power consumption in ALU helps us to realize low power processor. [3] Deals with the design and implementation of a Clock Gating Aware Low Power Arithmetic and Logic Unit that has been developed as part of low power processor. In [3], our designed ALU has 16 functions. Each function has one dedicated module. When one instruction executes in their respective module. Others module that was not used by current executing instruction must gated off by the clock gate. From given formula,

$$Power \ \text{Re} duction \ \% = \frac{Number \ \ of \ Unit \ \ Gated}{Total \ \ Number \ \ of \ Unit} * 100$$

Here, when any one of module execute because of clock gating rest 15 modules turned off and hence reduce power (15/16)*100=93.75% power reduction. Reference [4] reveals a large margin of potential for power saving based on clock gating functions that initially appear to be useless due to timing violation or excessive power consumption. Two optimization techniques is proposed in [4] for resurrecting such functions that can be used as a generic post-processing phase in an automatic clock gating tool. The first provides timing-aware approximation and the second aims at generating large gating domains by clustering similar clock gating functions.

III. RESULTS

A. Top-Level Schematic of 64-bit Register

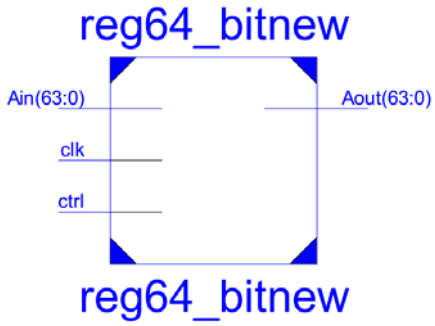

Figure5: Top Level Schematic of 64-bit Register

It has one 64-bit input Ain. Clock and control are two others outputs. It has one 64-bit output Aout. Register is a circuit which store information. This 64-bit register stores 64-bit inputs.

B. *RTL Schematic of 64-bit Register*

RTL is Register Transfer Level schematic. That display how this design will transfer on register in next phase of synthesis and implementation. It is based on native generic register (NGR) file. NGR was earlier EDIF in electronics. It uses 65 D flip-flop and one AND gate.

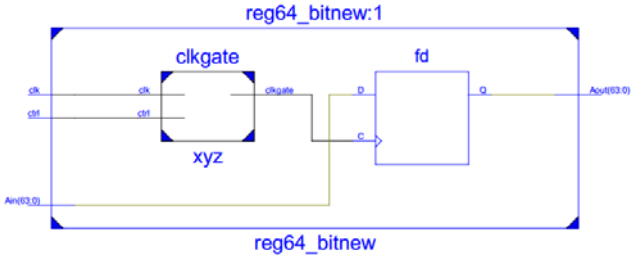

Figure6: RTL schematic of 64-bit Register

Depending on control condition clock gate will control the supply of clock to registers. When ctrl is high, then clock will be provided to register. Otherwise, we prohibit clock to register.

C. *Top Level Schematic of Clock Gate*

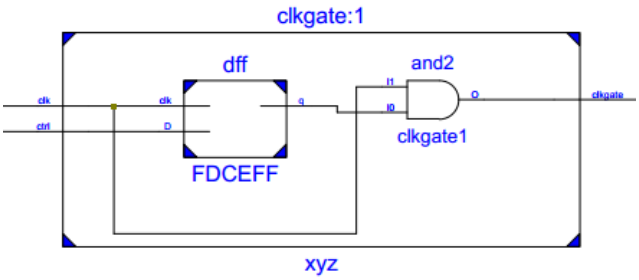

Figure7: Top Level Schematic of Clock gate

Clock gate is a combination of logic gate AND/OR and D Flip-Flop. First, D Flip-flop delay to reach control or enable to logic gate. Then the value of control or enable signal determine clock will be provided to register or not.

D. Technology Schematic of Clock Gate

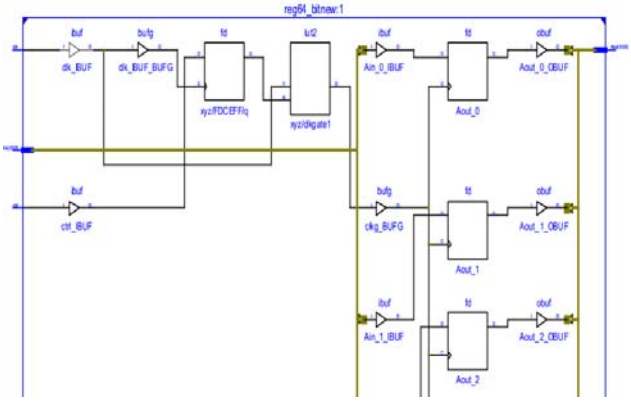

Figure8: Technology Schematic of 64-bit Register (a)

Above Figure shows 4 Flip-Flops. One flip-flop is used in clock gate circuits. Three flip-flops is used in register circuits.

It consists of one LUT2, 65 D Flip-Flops, one in clock gate and 64 in registers. It has two global clock buffers. It has 130 buffers. Out of 130, 66 are input buffer and 64 are output buffers

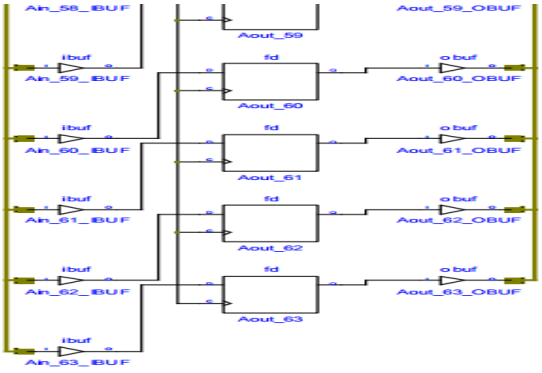

Figure9: Technology Schematic of 64-bit Register (b)

Technology Schematic is based on native generic circuit(NGC) file. It shows the netlist based on LUT and gate. This schematic has one two-input look up table.

E. Power Consumption

Power dissipation has two components. One is dynamic power and other is static power. In this analysis on XPower, dynamic power consists of clock power, logic power, signal power and IOS power. Static Power is also called Leakage Power.

Power Consumption with Clock Gate			
	15ps	2ns	15ns
Clock Power	1.351W	0.008W	0.002W
Logic Power	0.019W	0.000W	0.000W
Signal Power	0.505W	0.004W	0.001W
IOs Power	36.679W	0.132W	0.022W
Leakage Power	0.773W	0.043W	0.042W

Power Consumption is inversely proportional to clock period and directly proportional to clock frequency. It is maximum at 15ps clock period. It is minimum at 15ns.

F. Dynamic Current

It is the current, which our device takes, when our design register is in use.

Power Consumption with Clock Gate			
	15ps	2ns	15ns
Vccint	3.777A	0.020A	0.004A
Vccaux	1.996A	0.007A	0.001A
Vcc018	17.325A	0.062A	0.010A
Vccbram	0.000A	0.000A	0.000A

Dynamic current is affected by these above four voltages. These are Vccint, Vccaux, Vcc018 and Vccbram. Dynamic current is affected with minor variation in clock period.

G. Static Current

Static current is leakage current, which flow only when device is in off state. In real life, we face with this problem, when our mobile discharge after a couple of day, even if we don't use our cell phone.

Power Consumption with Clock Gate			
	15ps	2ns	15ns
Vccint	0.625A	0.017A	0.017A
Vccaux	2.063A	0.013A	0.013A

Vcc018	17.326A	0.001A	0.001A
Vccbram	0.025A	0.000A	0.000A

Static current is not affected with minor variation in clock period. Vccint is supply for the core unit. Vccaux is supply for the configuration pins and unit. Vcco is supply for the IO buffers.

H. Effect on Temperature

Junction Temperature with and w/o Clock Gating			
Junction Temperature	15ps	2ns	5ns
Without Clock Gate	125^0C	25.6^0C	25.2^0C
With Clock Gate	-----	25.9^0C	25.3^0C

Clock Gating is a technique, which decreases power consumptions but increases junction temperature.

I. Effect on Clock Gate

On 2 ns	With Clock Gate	Without Clock Gate
Clock Power	0.007W	0.008W
Signal Power	0.003W	0.004W
Total Power	10mW	12mW

We achieve 16.66% power reduction in 64-bit Register when clock period is 2 ns in 64-bit register. In this way, we achieve our prime goal to reduce consumption of power in our design.

On 5 ns	With Clock Gate	Without Clock Gate
Clock Power	0.002W	0.003W
Signal	0.001W	0.001W

Power		
Total Power	3mW	4mW

We achieve 25% power reduction in 64-bit Register when we provide clock period of 2 ns to 64-bit register.

IV. CONCLUSION

16.66% clock and signal power reduction in 64-bit Register when we provide clock period of 2 ns to 64-bit register. 25% clock and signal power reduction in 64-bit Register when we provide clock period of 2 ns to 64-bit register. Power reduction is benefit of clock gating techniques but area is trade off of this technique which increases due to additional clock circuitry. Another trade-off is Temperature. Temperatures slightly increase with significant decrease in power consumptions.

V. FUTURE SCOPE

This implementation is on 40-nm Virtex-6 FPGA. Now, there is scope to implement clock gated sequential circuit on latest 28-nm Virtex-7, Artix-7 FPGA. There is a scope to implement clock gate on the larger circuit in order to reduce power dissipation in significant amount.

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