A DIFFUSION BASED LOW POWER CONSUMPTION APPROACH TO CONSTRUCT 90NM FULL ADDER

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ABSTRACT

There is always the requirement of efficiency enhancement in each architecture. If the hardware based architectures are optimized, It will enhance the complete system. The proposed work is in same direction to reduce the power consumption in the construction of 90nm Full Adder with CMOS Architecture. This paper presents the filtration approach for high performance and low power architecture generation. In this proposed work the diffusion input scheme is introduce to reduce the power in digital circuits. The system will gives the concept of low power logic design that will use reduced layout area, less number of devices and the low power consumption. The proposed system will be implemented in Active HDL or in the ModelSim simulator. The simulation will be presented in the form of Waveforms. The work will be independent to the layout.

Keywords: *Full Adder, Power Reduction, Active Hdl, CMOS, Architecture, Digital.*

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I INTRODUCTION

Finite impulse response (FIR) filters are important building blocks for various digital signal processing (DSP) applications. Recently, because of the increasing demand for video-signal processing and transmission, high-speed and high-order FIR filters have frequently been used to perform adaptive pulse shaping and signal equalization on the received data in real time, such as ghost cancellation [2], source coding, equalizer, Partial-Response Maximum Likelihood (PRML) and channel equalization [7]. Signal processing algorithms often require a substantial amount of floating-point (or fixed-point) computations to be performed at real-time or near real-time speeds. Hence, an efficient VLSI architecture for a high-speed FIR filter is needed. FIR digital filters have been and continue to be one of the fundamental processing elements by virtue of stability and easy implementation. However, the large number of involved multiplications leads to excessive hardware complexity and power consumption. The FIR filter is composed of multiplications and adders. The performance of multiplications and adders determines the speed of FIR filter is represented by the following equation.

$$Y(n) = \sum_{k=0}^{N-1} x_k \, h_{n-k} - - - (1)$$

Most of the Very Large Scale IC (VLSI) applications, such as digital-signal processing and microprocessors, use arithmetic operations extensively. In addition, among these widely used operations, subtraction and multiplication are most commonly applied. The 1-bit full adder is the building block of these operation modules. Therefore, enhancing its performance is crucial to ameliorating the performance of overall modules. Meanwhile, as the widespread use of portable IC devices, such as MP3 players, mobile phones and PDAs etc., IC engineers are required to improve the performance of existing operation modules in some aspects, especially in power depletion and size. Since the battery technology available does not advance at the same rate as the microelectronics technology, IC designers have encountered more constraints: high speed, high throughput, small silicon area, and at the same time, low power dissipation. Hence, the research of establishing low power, high performance adder cells is becoming feverish. One efficient method to accomplish this task is derived from the structural level. This approach to designing and analyzing an adder cell is decomposing it into smaller modules for further analysis and improvement. In this way, an optimized full adder cell can be constructed by connecting these improved smaller modules.

There are two basic approaches to reduce power consumption of circuits in scaled technologies: reducing the dynamic power consumption during the active mode operation of the device and the reduction of leakage current during the stand-by mode. The power consumption of a CMOS digital circuit can be represented as

$$P = f C V_{DD}^2 + f I_{short} V_{DD} + I_{leak} V_{DD}$$

Where,

F - Clock frequency

C - Average switched Capacitance per clock cycle

V_{DD} - The supply voltage

I_{short} - Short circuit current

I_{leak} - Leakage current.

II LITERATURE SURVEY

A new low-voltage high performance CMOS I-bit full adder circuit is proposed. The new design is derived by combining XOR (XNOR) gatcs used in the conventional full adder [I] and transmission gates developed in [Z]. The proposed full adder can provide full voltage swing **at** a low supply voltage and offers superior performance in both power and speed than the conventional full adder [I], the transmission full adder [Z], and thc low-voltage full adder 131[9]. The sum and carry generation circuits of the proposed full adder are designed with hybrid logic styles. To operate at ultra-low supply voltage, the pass logic circuit that cogenerates the intermediate XOR and XNOR outputs has been improved to overcome the switching delay problem. As full adders are frequently employed in a tree structured configuration for high-performance arithmetic circuits, a cascaded simulation structure is introduced to evaluate the full adders in a realistic application environment. A systematic and elegant procedure to scale the transistor for minimal power-delay product is proposed. The circuits being studied are optimized for energy efficiency at 0.18- mCMOSprocess technology. With the proposed simulation environment, it is shown that some survival cells in stand alone operation at low voltage may fail when cascaded in a larger circuit, either due to the lack of drivability or unsatisfactory speed of operation. The proposed hybrid full adder exhibits not only the full swing logic and balanced outputs but also strong output drivability. The increase in the transistor count of its complementary CMOS output stage is compensated by its area efficient layout. Therefore, it remains one of the best contenders for designing large tree structured arithmetic circuits with reduced energy consumption while keeping the increase in area to a minimum[10]. With the characteristics of full voltage swing at internal

nodes and very low short circuit current, HSPICE and Nanosim simulations shown that the proposed full adder offers a power-delay improvement of 36% over the best of other 1-bit full adders that were compared. A 0.35µm CMOS technology and a power supply of 3.3.V were used to simulate these adders. When used to build an 8-bits carry-ripple adder, the proposed full adder offers power savings up to 28% respect to the other ones[11]. By using hybrid various CMOS and pass transistor logic (PTL) design approaches, two novel low-power full-swing full adder cores with output driving capability are proposed for high-performance embedded structure. The main design objectives for these full adder cores are providing not only low power and high speed but also full-swing operation at a low supply voltage and the driving capability. The simulation results show that the proposed full adder core (design-1) is superior to other designs. It consumes 17.69% to 36.21% less power than three previous designs excluding 7.87% penalty than CMOS scheme, while it is 1.88% to 53.64% faster for sum and 11.64% to 40.67% faster for carry-out than all reference full adders[12].

Compared with other lowgate count full adder designs using pass transistor logic, the proposed design features lower operating voltage, higher computing speed and lower energy (power delay product) operation. The design adopts inverter buffered XOR/XNOR designs to alleviate the threshold voltage loss problem commonly encountered in pass transistor logic design. This problem usually prevents the full adder design from operating in low supply voltage or cascading directly without extra buffering. The proposed design successfully embeds the buffering circuit in the full adder design and the transistor count is minimized. The improved buffering helps the design operate under lower supply voltage compared with existing works. It also enhances the speed performance of the cascaded operation significantly while maintaining the performance edge in energy consumption. For performance comparison, both dc and performances of the proposed design against various full adder designs are evaluated via extensive HSPICE simulations[13]. The new hybrid full adder is composed of pass-transistor logic and static CMOS logic. The main design objectives for the full adder core are providing not only low power and high speed but also with driving capability. Using TSMC CMOS 0.35-µm technology, the characteristics of the experimental circuit compared with prior literature show that the new adder improves 1.8% to 35.6% in power consumption, 11.7% to 41.2% in time delay of *Co*, and 13.7% to 91.4% in power-delay product of *Co*. The circuit is proven to have the minimum power consumption and the fastest response of carry out signal among the adders selected for comparison. Due to the low-power and high-speed properties, both the new exclusive OR circuit and the new full adder can be efficiently integrated in a system-on-a-chip (SoC) or an embedded system[14].

A new structure of a hybrid full adder, namely, the branch-based logic and pass-transistor (BBL-PT) cell, which we implemented by combining branch-based logic and pass-transistor logic. Evolution of the proposed cell from its original version to an ultralow-power (ULP) cell is described. Quantitative comparisons of the optimized version, namely, the ULP full adder (ULPFA), are carried out versus the BBL-PT full adder and its counterparts in two well-known and commonly used logic styles, i.e., conventional static CMOS logic and complementary pass logic (CPL), in a 0.13*u*m PD SOI CMOS with a supply voltage of 1.2 V, demonstrating power delay product (PDP) and static power performance that are more than four times better than CPL design. This could lead to tremendous benefit for multiplier application. The implementation of an 8-bit ripple carry adder based on the ULPFA is finally described, and comparisons between adders based on full adders from the prior art and our ULPFA version demonstrate that our development outperforms the static CMOS and the CPL full adders, particularly in terms of power consumption and PDP by at least a factor of two [15].

III PRELIMINARIES

A. Logic Equations for the Proposed Full Adders

The full adder operation equations presented below can be stated as follows: given the three 1-bit inputs *A*, *B* and *Cin* which calculate two 1-bit outputs *Sum*, for sum and *Cout*, for carry out.

$$Sum = A \oplus B \oplus Cin \quad (2)$$

$$Sum = A \bar{\oplus} B \bar{\oplus} \quad (3)$$

$$Sum = (\bar{C}. \quad \oplus)) + (\quad C. \quad \bar{\oplus})) \quad (4)$$

$$Cout = (A.(A \bar{\oplus}) + (\quad C. \quad \oplus)) \quad (5)$$

$$(\quad B. \quad \bar{\oplus})) + (\quad C. \quad \oplus))$$

B. Redesigned XOR Gate

As shown in the equations above, XOR gate are the essential parts in full adders. The authors provide two diverse pairs of XOR gate to improve the performance of full adders. All these gates are implemented with CMOS transistors. The obvious advantages of small transistor number and special structures make them better alternatives for future uses. The major aim of using these newly designed XOR gate is to reduce power consumption in CMOS full adders.

1) XOR gate based on Gate-Diffusion-Input Cell

The Gate-Diffusion-Input (GDI) method is based on the use of a simple cell as shown in Figure 1. One may be reminded of the standard CMOS inverter at the first glance of this

circuit, but there are some important differences: (1) The GDI cell contains three inputs—*G* (common gate input of NMOS and PMOS), *P* (input to the source/drain of PMOS), and *N* (input to the source/drain of NMOS). (2) Bulks of both NMOS and PMOS are connected to *N* or *P* (respectively), so it can be arbitrarily biased in contrast to CMOS inverter. The basic GDI cell is shown in Figure 1.

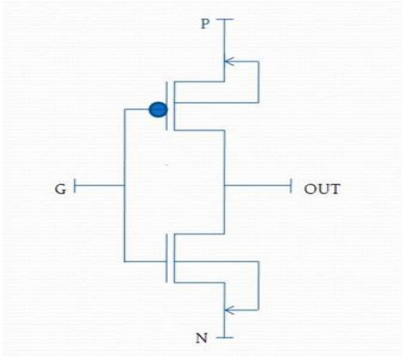

Figure 1. Basic Gate-Diffusion-Input cell

The GDI cell with four ports can be recognized as a newly multifunctional device, which can achieve six functions with different combinations of inputs *G*, *P* and *N*. TABLE I. shows that simple configuration changes in the inputs *G*, *P*, and *N* of the basic GDI cell can lead to very different Boolean functions [5] at the output *Out*. Most of these functions are complex (usually consume 6-12 transistors) in CMOS, while very simple (only 2 transistors per function) in the GDI design methodology.

Table I. Functions of The Basic GDI Cell

Input			Out	Function
P	*G*	*N*		
B	A	0	$\overline{A}\cdot B$	F1
1	A	B	$\overline{A}+B$	F2
B	A	1	$A+B$	OR
0	A	B	$A\cdot B$	AND
B	A	C	$\overline{A}\cdot B+A\cdot C$	MUX
1	A	0	$\overline{A}$	NOT

The XOR gate based on GDI cells are applications of the GDI technique. As can be seen in Figure 2, The XOR gate requires only four transistors. Obviously, the proposed GDI XOR gate use less transistors compared with the conventional CMOS counterparts. Due to some attractive features which allow improvements in design complexity, transistor counts, static power dissipation and logic level swing, research on GDI is becoming feverish in VLSI area. However, the GDI scheme suffers the defect of special CMOS process, specifically; it

requires twin-well CMOS or silicon on insulator (SOI) process, which are more expensive than the standard p-well CMOS process.

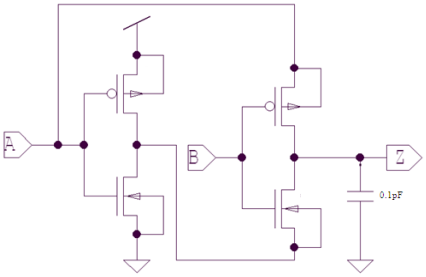

Figure 2. GDI EXOR gate

IV THE PROPOSED LOW POWER SYSTEM

A. Full Adder Based on Gate-Diffusion-Input Technique

According to the logic equations mentioned above and the GDI XOR gates in Figure 2, full adders can be redesigned in GDI XOR full adder. The proposed full adder in Section III.A includes ten transistors. Compared to the conventional CMOS logic full adder [4] uses 46 numbers of transistor. Since less transistors are used in GDI circuits. As is well known, the number of transistors in circuits can influence performance in many aspects, especially power.

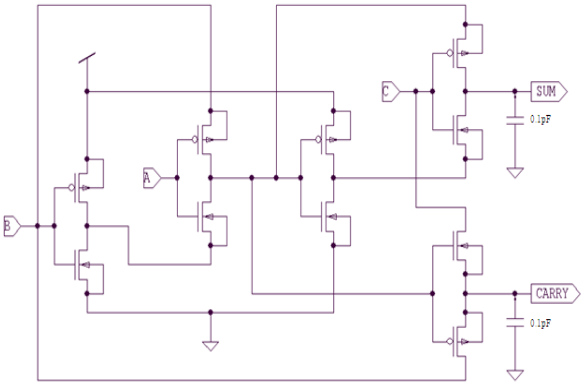

Figure 3. GDI EXOR Full Adder

The transistor level implementation of GDI XOR full adder is shown in Figure 3. This full adder consists of three modules-two GDI XOR gates and a multiplexer. The *Sum* and *Cout* can be calculated using (2) and (5). In the worst case, *Sum* has 4-T delay while *Cout* has 3-T delay. However, due to the advantages of GDI cell, this circuit still can achieve its benefit of low power consumption.

A ripple carry adder can be constructed using 4 full adder circuits connected in parallel as shown in figure 4. The carry output of each adder is connected to the carry input of the next

higher-order adder. Here, for least significant position, carry input of full-adder is made zero. A single full adder is capable of adding two one-bit numbers and an input carry. In order to add a binary numbers with more than one bit, additional full adder must be employded.

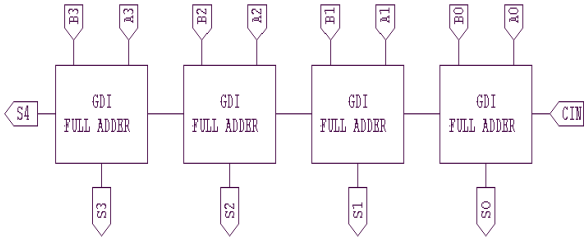

Figure 4. GDI Ripple Carry Adder

V CONCLUSION

In this paper, we have presented low-power realization of FIR filters are proposed. The newly designed modules possess the merits of low power dissipation, and area saving due to lower transistor counts and special structures. Different blocks were designed using GDI technique namely XOR logic gate, Full Adder. The blocks were designed also using conventional Complementary Metal Oxide Semi-Conductor (CMOS) logic.

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