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A NUMERICAL APPROACH OF ANALOG PHASE LOCKED LOOP MODEL FOR THE MULTIPLEXING OF MESSAGE SIGNALS

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Abstract

An analog phase-locked loop presents several challenges to designers in an all-digital design environment. Some all-digital simulators, such as Verilog XL, cannot represent analog signals easily. System designers must either use a mixed-mode simulator to represent the analog portions of the phase-locked loop, or use a simplified model of the phase-locked loop. In ASIC production test, limitations of the production test equipment must be taken into account. For example, an analog measurement may take a long time to complete. Also, functional testers cannot measure frequency, so it is difficult to determine that the phase-locked loop is operating properly in production test.

1. ESTIMATION FOR APLL MODEL

The block diagram of the proposed linear APLL model is shown in Fig.1.1. The multiplier performs a mixing operation between the input reference and VCO signals. Now, the PD is a signal multiplier and it has sinusoidal characteristics. If the PLL is initially in unlocked state then with little trigonometric manipulation, the output of the multiplier can be expressed as:

$$x_1(t) = A_1 \cos\big(\omega_1(t)\big) + \theta_1 \quad (1)$$

$$x_0(t) = A_0 \cos\big(\omega_0(t)\big) + \theta_0 \quad (2)$$

Where $A_1$and $A_0$are the amplitudes, ω_1 and $\omega_0$are the angular frequencies and *6,* and $\theta_c$are the phase constants of reference input and VCO output respectively.

The LF removes the high frequency component $\omega_i + \omega_0$ from multiplier output.

The VCO output signal x0(t) becomes synchronous with the input signal *x,(t)* after sufficiently long time of transient. Then, the signal *x0(t)* can be expressed as:

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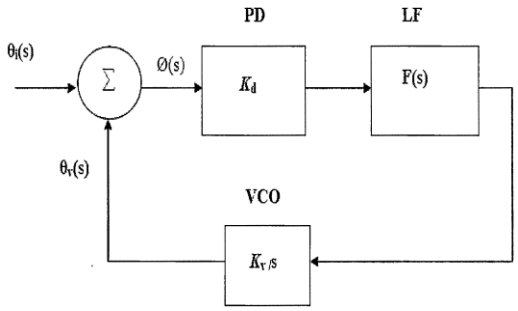

Fig.1.1: The proposed linear APLL model

The instantaneous angular frequency *comst* of the VCO is a linear function of the LF output or control voltage vc with reference to the VCO free-running angular frequency *a>o* and the VCO produces a sinusoidal signal. Deviation of VCO output frequency from its free running angular frequency *a>o* can be expressed as *KvvCt.* The frequency of oscillation of the VCO changes by *Kv* radians/sec for every volt of vc(0 applied as input to the VCO.

As the frequency is the derivative of phase, so we can write,

$$\omega_{mst} = \frac{d}{dt}(\omega_0 t + \theta_c) = \omega_0 + \frac{d\theta_c}{dt} = \omega_0 + K_v v_c(t)$$

Now, the change of VCO frequency ω_0 to ω_{inst} is due to $k_v v_c$ i.e.

$$\frac{d\theta_c}{dt} = K_v v_c$$

Eq. shows that due to the dc signal V_c, the VCO frequency is changing from its free running angular frequency a)0to the reference input angular frequency ω_0.

2. ESTIMATION FOR APLL MODEL WITH LAG-LEAD LF

It is not possible to adjust BW, loop gain, and damping independently with a simple RC filter as shown in Fig.9. This filter may be modified by connecting a resistor Ri as in Fig.3.2. This filter circuit is known as lag-lead LF. This is the most common type of LF that is normally used in linear PLL system. The second-order PLL with a lag-lead LF is commonly used because the lag-lead LF has two time constants to determine the natural frequency and the damping factor independently. A high speed PLL typically uses a simple lag-lead LF of first order, constructed from passive elements. This passive lag-lead LF is preferred in view of its circuit simplicity and noise performance in high frequency. This type of filter has the TF given by,

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$$F(s) = \frac{sCR_2 + 1}{sC(R_1 + R_2) + 1}$$

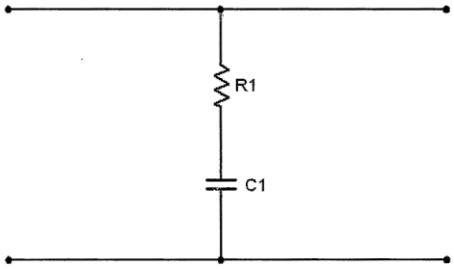

Fig. 1.2: Simple RC filter

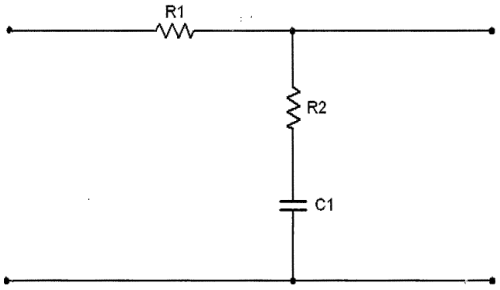

Fig.1.3: The lag-lead LF

$$= \frac{\mathbf{1} + \boldsymbol{\tau_2 s}}{\mathbf{1} + \boldsymbol{\tau_1 s}}$$

Where $\tau_1 = (R_1 + R_2)C$ and $\tau_2 = R_2C$ are time constants.

In most of the application, resistor $R_1 > R_2$so that $\tau_1 \gg \tau_2$. The high frequency asymptotic response of this lag-lead filter is given as $F(\infty) = {}^{\tau_2}/_{\tau_1}$

The closed loop TF of the linear APLL can be expressed as [8]:

$$\frac{\boldsymbol{\theta_V(s)}}{\boldsymbol{\theta_1(s)}} = \frac{\boldsymbol{K_v K_d F(s)}}{\boldsymbol{s} + \frac{\boldsymbol{K_v K_d F(s)}}{\boldsymbol{s}+}}$$

Whereω_n =, the natural frequency and ξ, the damping factor (DF) are defined as:

If,

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$$\zeta = \frac{\tau_2}{2}\left(\frac{K_v K_d}{\tau_1}\right)^{1/2}$$

$$= \frac{\tau_2}{2}\omega_n$$

ζ And ω_n have been extensively studied in various literature and their effects on the characteristics of PLL have been thoroughly documente**d**. The DF is a function of PLL gain and LF time constant. The natural frequency con is a function of Kd, which is, in turn, a function of input amplitude. These two parameters are important to characterize a PLL.

The highest power of s in the denominator of the closed loop TF is 2 and so the loop is known as second-order loop. The PLL model with a passive lag-lead LF is Type I in view of the presence of the perfect integrator in the VCO.

If the condition $K_v K_d \gg \omega_n$ is true, this PLL system is called a high-gain loop.

As all PLLs are usually designed to have high gain there is no true loss of generality for making this assumption. This is because a high loop gain makes the loop BW and DF relatively insensitive to variations in the gains. Most of the practical PLLs are having high-gain loops for good tracking performance. In practice, for a fixed loop gain *Kv,* the natural frequency con of the loop may be chosen and will be dependant mainly on τ_1, since $\tau_2 \ll \tau_1$ in most of the cases. So, according to Eq. (34), DF may be determined by τ_2 and for all practical purposes it will be an independent adjustment.

3. ESTIMATION FOR DYNAMIC RANGES

The dynamic ranges are related to acquisition mode of a PLL when its output is either out of lock or just starting to lock with the reference input. It means that the output of PLL is not locked or synchronized in phase and frequency with the reference input signal. The formulae for various dynamic range of acquisition such as lock-in, pull-in and settling time of PLL have been analyzed mostly for first order PLL and these have been approximated for second order PLL using lag-lead LF.

At higher frequencies the loop gain of a second order APLL with lag-lead LF can be expressed as:

$$K \approx K_v K_d F(\infty)$$

Where $F(\infty)$ is known as high frequency asymptotic response of lag-lead LF. For lag-lead LF, $F(\infty) = \tau_2/\tau_1$ where $\tau_1 = (R_1 + R_2)C$and $\tau_2 = R_2 C$. The ACOL for a second order APLL with lag-lead LF is approximately estimated as:

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$$\Delta\omega_L \approx \boldsymbol{K_v K_d F(\infty)}$$

The lock-in time is the transient time required for the PLL to lock into from the $\Delta\omega_L$ a first order PLL, $\Delta\omega_L$ is equivalent to IQ, of the loop. But for a second or higher order loop, $\Delta\omega_L$ is always less than IQ, of the loop. There is a frequency range, which is smaller than dc gain (IQ,) but larger than $\Delta\omega_L$ over which the PLL will lock after slipping cycles for a while. This range is known as pull-in range. If the initial frequency difference is very large or the LF output is very small, then the loop cannot pull in. The maximum frequency range for which the loop can still lock is known as Acop. An approximate formula, which is applicable for the condition $K_v \gg K$ for $\Delta\omega_p$ can be written as:

$$\Delta\omega_p \approx \sqrt{2\boldsymbol{K_v K_d K}}$$

Pull-in time (Tp) is defined as the time required for pulling from the initial offset to ACOL when the loop locks quickly. If $\Delta\omega \gg K$ K, then Tp can be approximated as:

$$T_p \approx \frac{(\Delta\omega)^2 \boldsymbol{\tau_2}}{K^2}$$

This formula is not well approximated if $\Delta\omega_L$ is either very large (near$\Delta\omega_p$) or very small (near $\Delta\omega_L$). **Fig.1.4** shows a graphical view of $\Delta\omega_L$ and $\Delta\omega_p$ values with reference to VCO free running frequency.

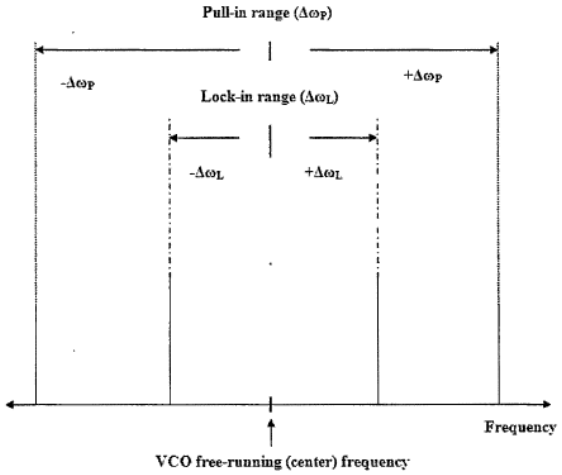

Fig. 1.4: The graphical representation of PLL dynamic ranges

4. ESTIMATION FOR LOOP BW

The LF characteristic plays an important role in determining the performance of the PLL. Narrow

LF BW results better noise but in expense of slow locking time. On the other hand wide LF BW results fast locking time but at the cost of noisy VCO output. The aim of PLL designer is to provide optimum locking time for the selected LF BW. The acquisition time is linearly proportional to the loop noise BW. The loop noise BW is proportional to the loop gain of the PLL. So, when the loop gain is large, the acquisition time will be short. But the large loop gain makes the PLL noisy and it causes the PLL to unlock.

The loop noise BW can be expressed as

$$B_L = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right)$$

In most of the cases C « l/KvKd, so, all the left most terms of both numerator and denominator may be ignored and the expression can be re-written as:

$$B_L = \frac{1}{4C(R_1 + R_2)}$$

Eqshows that the loop BW can be closely estimated from the LF component values and the value of loop B W is approximately equal to one fourth of the comer frequency of the LF, as long as the capacitance is small compared to the reciprocal of the loop gain [54]. This can be calculated as the reciprocal of the sum of the resistances multiplied by the capacitance.

5. ESTIMATION FOR INPUT SNR

The SNR is useful engineering concept for defining performance parameter of PLL. The input SNR is the ratio of input signal power to input noise power. The estimation of input SNR is made by using simulation technique for generating WGN samples with good statistical properties using random number function to make an accurate estimate of the effects of noise on PLL performance. The Gaussian PDF of Gaussian noise distribution is defined for a continuous random variable *x* as:

$$p_x(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-(x-m)^2}$$

In Eq.(43), *m* is the mean of the random variable and a is the standard deviation of the random variable.

The AWGN

We impose AWGN source on our proposed APLL model to study the effects of noise. The reference input to the PD of the model is shown in Fig.1.5. It consists of the sinusoidal signal *x,(t)* plus the AWGN *n(t)*.

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The AWGN can be expressed as:

$$x_r(t) = x_i(t) + n(t)$$

Linear behaviour

If the input noise to the loop is sufficiently small i.e. the phase error disturbance is small enough, the sinusoidal non linearity of the PD can be neglected. The input SNR can be defined as

$$SNR' = \frac{A_r^2}{2\sigma^2}$$

Where A, is amplitude of the reference input signal as given in Eq.(l) and a2 is the variance of the AWGN samples. The phase error variance of PLL is approximated as:

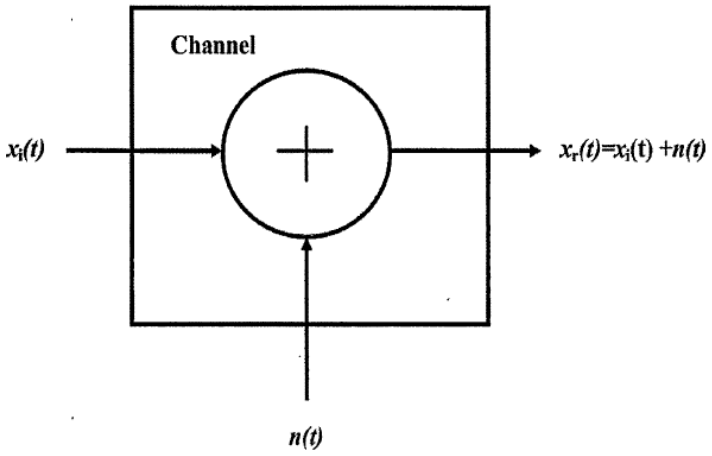

Fig.1.5: The AWGN channel

Non-linear behaviour

The phase error in PLL may not be in its linear region of operation when the SNR is very low. The PLL with a noisy reference, a noise-induced cycle slip is said to have occurred when the phase error 0 increases or decreases by *2%* radians after the PLL starts from a stable equilibrium point. Cycle slips in PLL are nonlinear phenomena. As such, mathematical analyses of cycle slips are considered to be extremely difficult. In this non-linear situation, the modulo-27t phase error process is used to describe the steady-state PDF by using the steady-state solution of Fokker-Planck equation at different values of input SNR.

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6. ESTIMATION FOR LF USING COMPANION MODEL

The LF used for the present work is of lag-lead type as shown in Fig.1.6. The charge-storage element of the LF is simplified to an equivalent linear companion model by transient analysis method. The circuit simulator tools like SPICE has usually used the companion network models for time domain analysis. A capacitor is transformed by using a two step process. The first step is by applying numeric integration to the current-versus-voltage relationship of a capacitor. The nextstep is by applying the result to develop the linear companion model suitable for nodal analysis. The differential equation for current-versus-voltage relationship of a capacitor can be expressed as:

$$i_c = C\frac{dv_c}{dt}$$

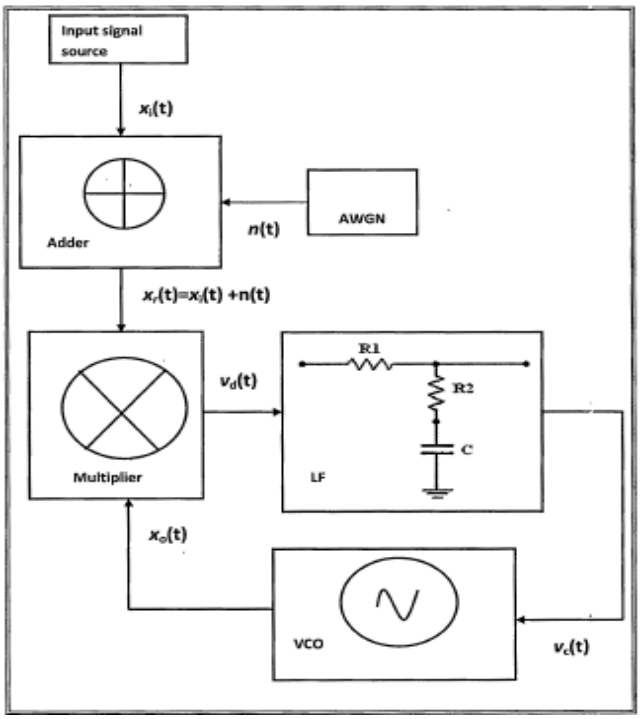

Fig.1.6: The proposed model with AWGN source

This derivative is approximated numerically by using numeric integration known as Backward Euler method. Backward Euler method offers a good compromise of accuracy and stability.

$$t^{n+1} - t^n = T$$

Where, T is called the step size. The calculation of T by using Backward Euler numeric integration

technique is shown in **Fig.1.6**

The current, ic(n+1) is an approximation to the true capacitor current. The branch representation for a capacitor in the companion model follows from Eq.(51) by the application of Kirchhoff s Current Law (KCL) at a node as shown. In searching for a solution, the program iterates on node voltage values over and over again until a set of voltages is found that satisfies the KCL. Conductance G describes the part of C's current dependent on its new voltage v*(n+I).* Current source *Ieq~ G.v* n describes the other part based on the past voltage. Since vn is the node voltage from previous time step and remains fixed, only *v(n+l)* changes with each new iterative voltage value and 4(n+1) changes to become the linear I-V relation for the new capacitorVoltage at that transient time point. The value of the resistors Rj and R2 of the LF are represented by its conductance value in the system matrices. The nodal equations for LF are represented in a set of matrices as [G] [V]=[I]. This matrix characterizes the linear representation of the voltage and current for the LF circuit at each discrete time point.

7. CONCLUSION

This paper presents modeling of one of the building block of a communication and a tracking system, a general purpose analog PLL IC LM 565, by introducing a new concept of combinational modeling. Wherein, modeling phase detector at primitive level improves accuracy, and VCO is modeled using ABM technique that results in increasing speed, a great deal. The cascading of PD & VCO outputs has overall effect to augment accuracy, and speed is now comparable to behavioral model of PLL. The loop filter being a simple RC circuit can be modeled either by using ABM method or using PSpice primitives, and doesn't affect simulation speed. Moreover, phase detector modeled mimics the IC behavior in silicon. . The model works out to the specifications.

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