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THE STUDY ON HIGH AND LOW-VOLTAGE MOSFETS INTEGRATION ON InGaAs

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ABSTRACT

Many electronic devices may benefit from higher performance and greater efficiency if high and low-voltage MOSFETs were integrated on InGaAs. Due to its better electrical characteristics compared to silicon, MOSFET integration on InGaAs has been a focus of study. MOSFETs are the most often utilized transistors in power electronics. More efficient and faster electronic devices for a wide range of uses might result from a deeper knowledge of the design, manufacturing, and characterization of both low and high-voltage MOSFETs on InGaAs, which is the focus of this research. This research investigates the integration of high- and low-voltage MOSFET on InGaAs.

Keywords:MOSFETs, InGaAs, transistors, power electronics, silicon.

1. INTRODUCTION

Smart PICs have been developed thanks to the combination of power stages with low-voltageanalog and digital circuitry. The benefits of smart power ICs in modern electronic systems include reduced size, weight, and cost as well as enhanced performance and reliability; this is in addition to reduced power consumption and reduced interface functions. In addition, the development of low-power RFICs has been spurred by the rising expectations placed upon practical electronic systems. [1]

Power consumption is cut down, isolation is increased, dependability is increased, and more small-signal analog or digital devices may be integrated with power devices, SOI technology is the technology of choice for these circuits. By reducing the MOSFET's physical dimensions, ft, and fmax have been attained up to many tens of GHz, making it suitable for use in small-signal applications despite its high current capacity and low capacitance. Power high voltage MOSFETs with breakdown voltages in the 30-80 V

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range, on the other hand, see the extensive application in RF power integrated circuits. To accommodate the gigahertz radio frequency signal, these devices typically have a gate length of 0.3 to 1.0 m and a gate-oxide thickness of several tens of nanometers.[2-3]

Although silicon's excellent quality and thermodynamically Sio_2 have made it a popular choice for electronic device manufacturing, the performance of Si-based devices is reaching its limitations owing to features such as sluggish mobility. As a result, non-Si materials are required to boost the functionality of electronic devices, especially at high frequencies. Due to their improved transport capabilities, III-V based semiconductor materials have recently attracted a lot of interest from the scientific community. [4-6]

Over the last two decades, InGaAshas gained traction as a possible silicon replacement for use in cutting-edge, high-speed digital gadgets of the future. The lack of a readily available native oxide, analogous to silicon's Sio_2, posed a significant challenge for InGaAs production. In the past, several attempts were made to perfect the InGaAs MOSFET production process by using better insulators. [7-8]

These studies prove that increased drive current, decreased access resistance, and enhanced transconductance may result from increased carrier mobilities and decreased effective masses. The investigation of InGaAs as a material for high-voltage power supplies was equally fascinating. Some findings in the literature show that power MOSFETs may benefit from high mobility InGaAs semiconductors in terms of improved performance (increased Vbr,Vbr is defined as the VDS at which ID is greater than $10x^{12}$ A/µm,and ID, decreased Ron,sp, greater gm, better frequency responsiveness, and larger SOAs). Therefore, this chapter's goal is to investigate high- and low-voltage MOSFET integration on InGaAs. Smart power ICs on InGaAs will benefit from this idea.[9-10]

2. MATERIAL AND METHODS

2.1 DEVICE STRUCTURE

The combination of a low-voltage MOSFET with a junction-isolated high-voltage DTG MOS-FET is shown in Fig. Both devices separate the drain contacts from the p-base and the source area with an oxide-filled trench and a vertical creation of n-channels in the p-base. At the same time, the current that drains flows in both directions, from the drain connection to the source contact. The oxide thickness plays a significant role in the extremely high voltage DTG

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MOSFET. t_{ox}=0.3 µm, and t_{ox1}=0.91 µm,and t_{ox2}=0.1 µm. The length of a cell pitch is 3 meters, while the length of a gate is 0.5 µmicrometers; L_1=0.6 µm, L_2=1.34 m, L_3=0.46 µm. Doping levels in the p-body are 8 x 10^{16} cm^3 and in the n-drift region are 1.5 x 10^{16} cm^3. Since the gates have more influence on ID when two channels are conducted through them at once, the ID and gm are improved. The high voltage DTG MOSFET has a greater ft and fmax when gm is large. Because of the improved RESURF effect, the drift area of a high-voltage DTG MOSFET is lengthened when it is folded in the horizontal and vertical directions, and the electric field is suppressed. This results in a greater V_{br}.

On top of the same InP substrate sits a layer of In0 53Ga0 47As with a doping concentration of 1 x 10^{19} cm^3, making up the low-voltage MOSFET. For ohmic source connections, we employ a 60 nm p-type In0 53Ga0 47As 95 layer with 2 x10^{18} cm^3 of doping and a 20 nm In0 53Ga0 47As n -cap layer with 1x 10^{19} cm^3 of dopinglayer, so reducing contact resistance by lowering the distance between the drain and the channel.The trench's Al_2O_3 blocks off the drain from the water supply. To keep the TaN gate electrode in place, a 2 nm-thick gate oxide is etched into a central trench. Improve gate control by shifting the SCEs by using a higher k dielectric material or reducing the oxide layer. If the gate potential in a vertical p-type InGaAs layer is increased over the threshold potential, then dual channels will form on both sides of the gate.

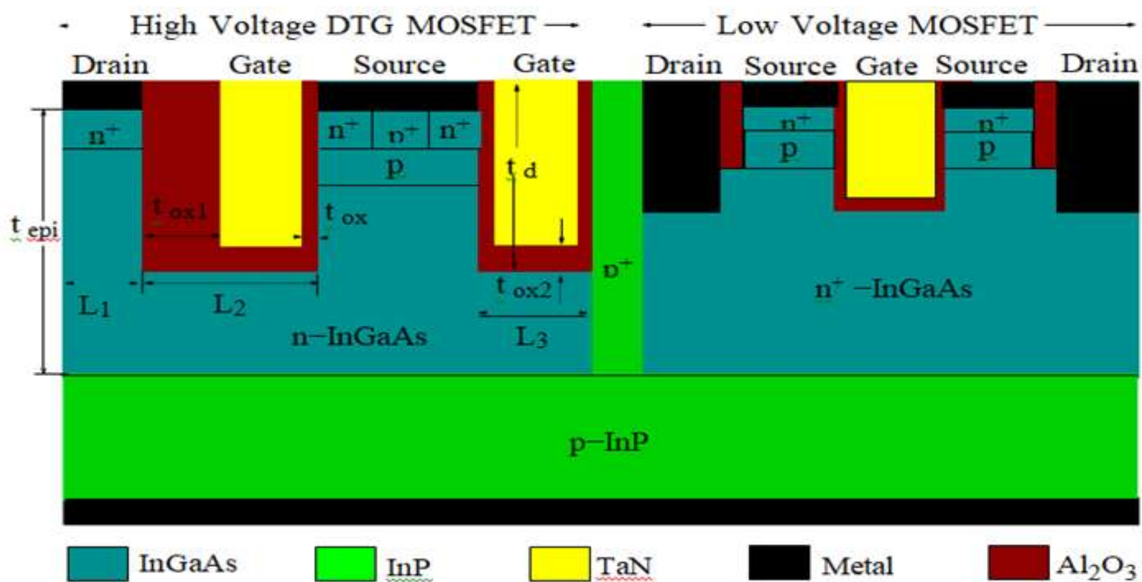

Figure1: **The isolated junction cross section of a high-voltage DTG MOSFET with a low-voltage MOS- FET.**

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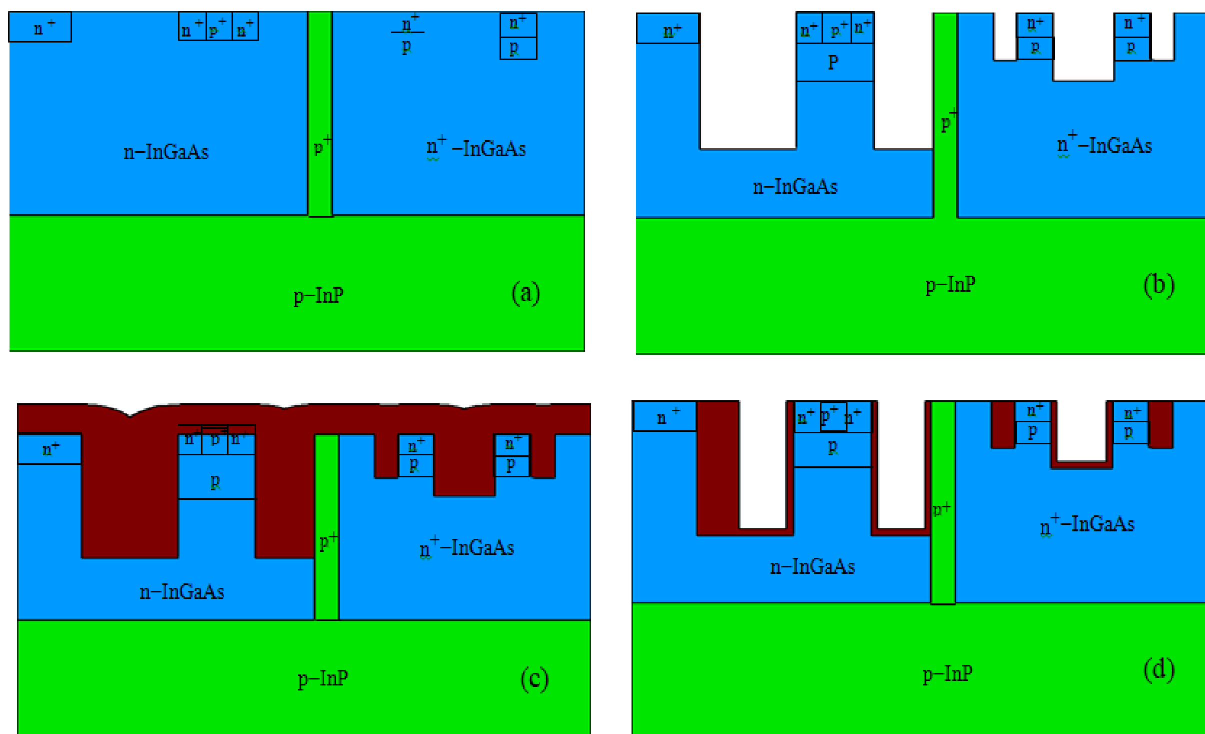
The gm or ID are both increased by simultaneous channel conduction, leading to a higher ft and fmax. The recommended method of producing both high- and low-voltage MOSFETs with a junction isolation barrier is shown in Fig. ATHENA is used as a design tool for the fabrication process. “In this process, an n-InGaAs layer 2.2 m thick is produced on top of an InP substrate with a doped concentration of 1.5 x 10^{16} cm^3. The implantation of boron and BF2 results in p-base for both gadgets. The p or n zones are created by implanting ions of BF2 and arsenic. As can be seen in Fig.1, the high-voltage DTG MOSFET is sandwiched between the lower-voltage MOSFET and a layer of heavily doped InP. For the high-voltage DTG MOSFET, two trenches are created using two separate masks; whereas for the low voltage MOSFET, three trenches are created using three separate masks (see Fig.2). As can be seen in Fig.Al_2O_3 completely coats the substrate. Al_2O_3 is etched away as indicated in Fig. in order to achieve a tox of 30 nm in a high-voltage DTG MOSFET and 2 nm in low voltage MOSFET.” In Fig.2, you can see how TaN completely coats the substrate. As can be seen in Fig., a field plate is carved out of TaN at the bottom of gate trenches. InGaAs surface etching is seen in Fig.2. The last step in creating isolated junction connections is metallization and patterning.



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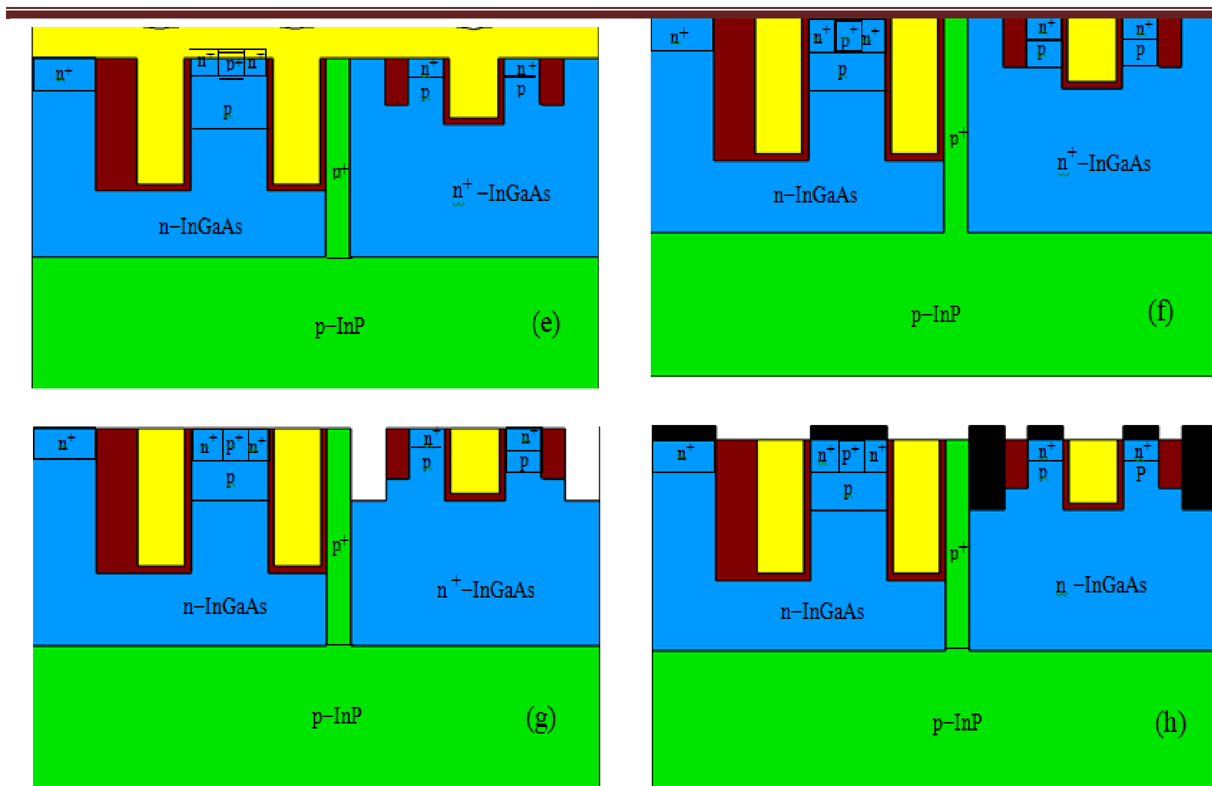

Figure 2:Construction Methods for Low Voltage MOSFETs and Junction-Isolated High Voltage DTG MOSFETs.

3. RESULTS&DISCUSSION

The SILVACO ATLAS software is used to do simulations of both high-voltage DTG MOSFETs and low-voltage MOSFETs with junction isolation, using either the CONMOB, Fermi-Dirac, FLDMOB, and CVT Lombardi models. At the InGaAs/Al_2O_3 interface, we account for Dit by assigning it a value of 1 x 10^{12} eV^{-1} cm^2. The features of a high-voltage DTG MOSFET's output are shown in Fig.3 across a VGS. At V_{DS} = 15 V and V_{GS} = 2 V, the ID of a high-voltage DTG MOSFET is 0.074 mA/ µm. The figure shows the output features of a low-voltage MOSFET with a gate voltage of varied strengths when used with an LG of 60 nm.Channel formation in low-voltage MOSFET results in an ID of 0.53 µmA/m at V_{GS}=V_{DS}=1 V.High voltage DTG MOSFET transfer &transconductance characteristics are shown in Fig.4&5. At a constant current of 107 µA/ µm, Vt is determined to be 1.32 V. The DTG MOSFET's high gm is a result of the fact that both gates may manipulate the ID at the same time. The gadget has a maximum gm of 106 µS/ µm at a V_{GS} of 2.25 V.

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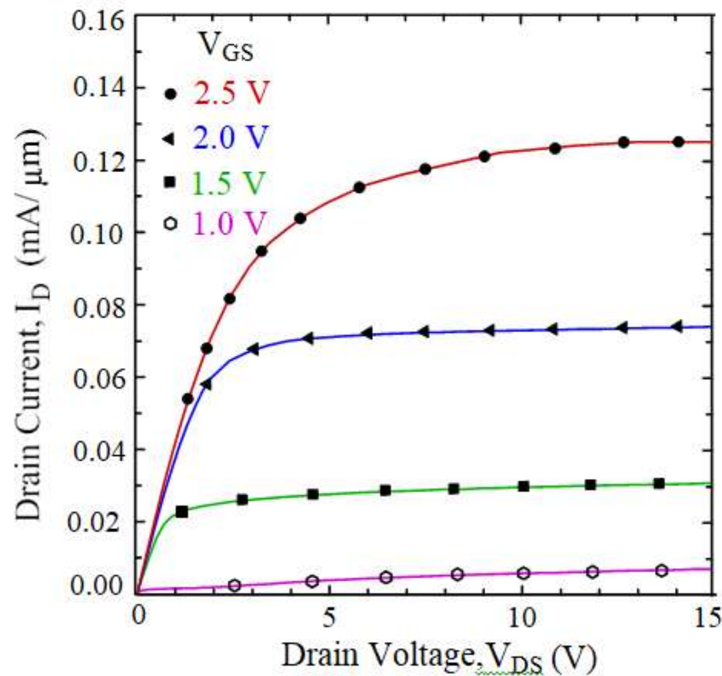

Figure3: High-voltage DTG MOSFET output characteristics.

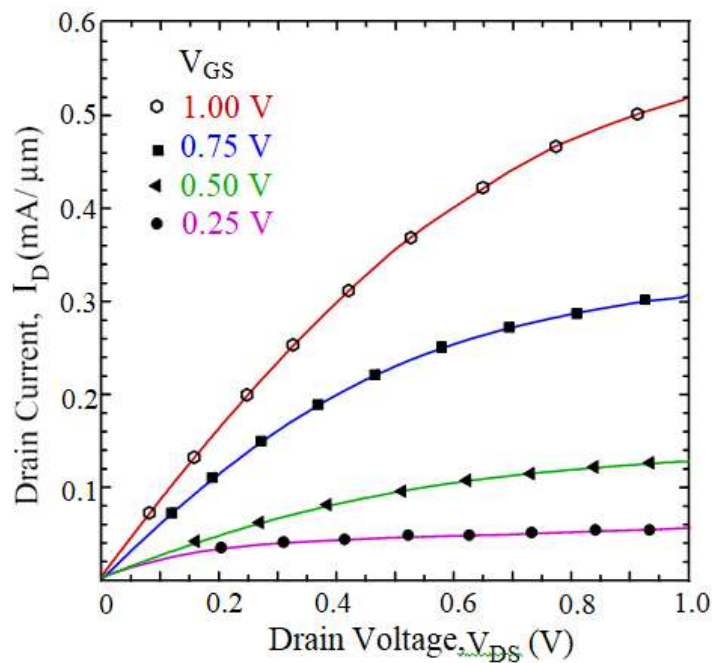

Figure 4: Features of the MOSFET's output at low voltage.

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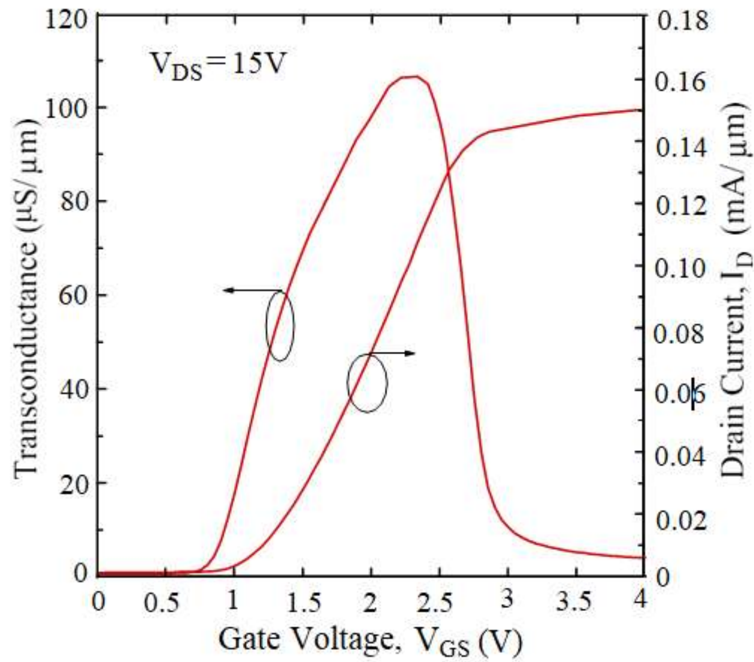

Figure 5: High voltage DTG MOSFET characteristics in terms of transfer and transconductance.

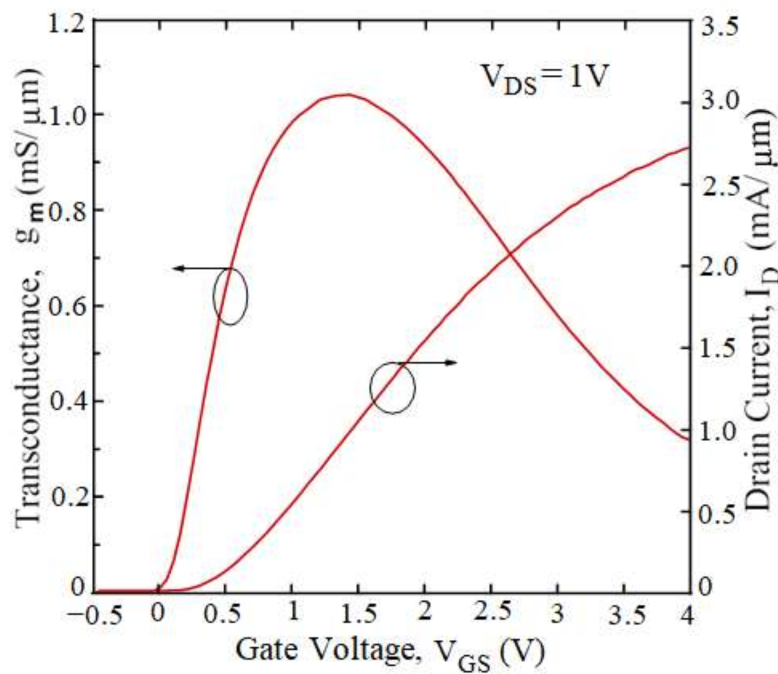

Figure 6: The low voltage MOSFET's transfer and transconductance properties.

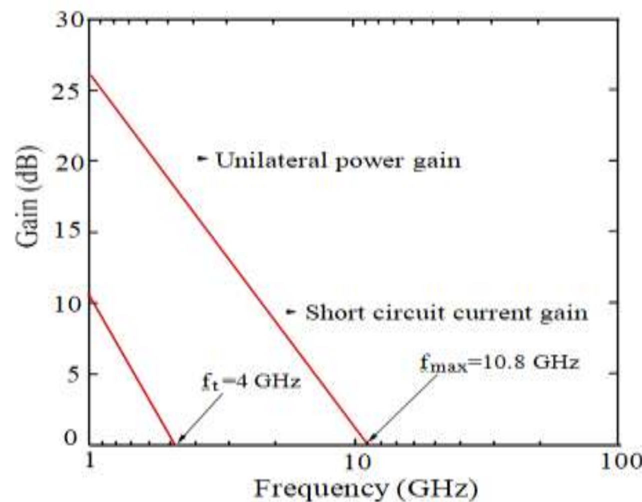

Figure 7: frequency dependence of the high-voltage DTG MOSFET's.

As can be seen in Fig.6 for a low voltage MOSFET, Vt equals 0.493 V, and max gm is attained at 1.35 V for a gate-source voltage of 1.033 µmS/ µm.Devices with a high gm are well-suited for use as RF amplifiers. The DTG MOSFET's microwave properties are shown in Fig.7 Eqipment's footing.

Whereas the highest frequency measured was 10.8 GHz. Capacitances at the gate and drain nodes were measured to be 0.6 fF/m and 8.08 fF/m, respectively.

The low voltage MOSFET's frequency characteristics are seen in Fig.8. The gadget has an ft of 44 GHz when the current gain is at unity. The increased gm of the MOSFET is responsible for the high value of ft.

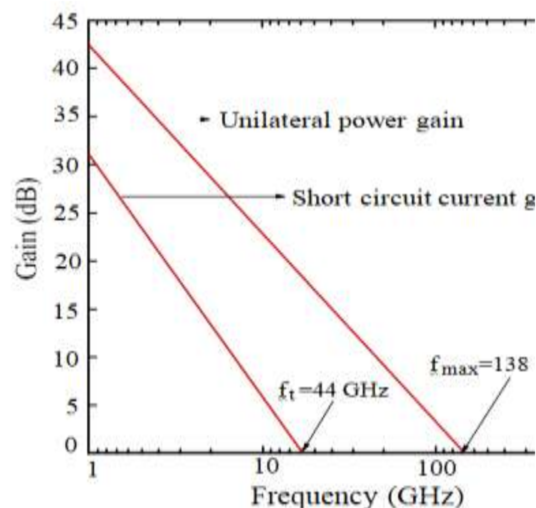

Figure 8: The low-voltage MOSFET's frequency response.

This low voltage MOSFET has a maximum frequency of 138 GHz. For the suggested MOSFET, the retrieved Cgs is 2.46 fF/ µm & the Cgd is 1.29 fF/ µm. In Fig.9, we see a plot of ft and fmax vs V_{GS} for the low voltage MOSFET. At V_{GS}=1.35 V, the device's ft and fmax are also at their highest.

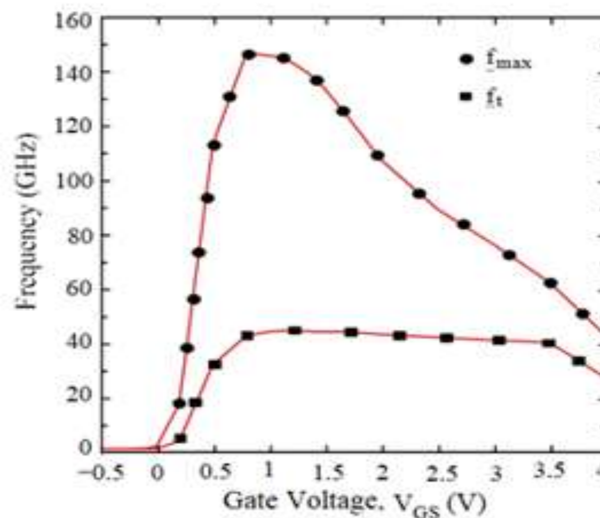

Figure 9:Changes in frequency with low-voltage MOSFET gate-source voltage

Sub-threshold behavior of the low-voltage MOSFET is seen in Fig.10. At V_{DS}=1 V, the structure's SS is 78 mV/dec for LG=60 nm. From this, we can determine that the MOSFET's DIBL is 118 mV/V. Small changes in V_t with V_{DS}, thanks to the trench gate's help in achieving greater control of the potential in the p-base, are responsible for the device's suppressed DIBL. Figure shows that at a V_{DS} of 1 V, the I_{ON} /I_{OFF} ratio of a low voltage MOSFET is 0.8 x 10^7.

The high voltage DTG MOSFET's breakdown characteristics at VGS=0 V are shown in Fig. 11. V_{br} is defined as the V_{DS} at which ID is greater than $10x^{12}$ A/µm. The trench structure's high V_{br} of 52 V is attributed to the reduction of the electric field in the drift layer.

$R_{on, sp}$, and V_{br} for the high voltage DTG MOS- FET are shown to be Nd-dependent in Fig.12. Since the depletion layer covers the whole drift zone, the peak magnetic field within the device is reduced to 52 V for N_d=1.5 10^{16} cm^3, as seen in Fig12. Due to the fact that the drain side of the drift region is not completely depleted, the number of field lines within the drift zone increases when N_d> 1.5 x 10^{16} cm^3. Fig.13, demonstrates that when Nd increases, resistance within the drift zone decreases, leading to a decrease in $R_{on, sp}$.

The MOSFET offers the best compromise between V_{br} and $R_{on,sp}$.Fig. 13, Shows how $R_{on,sp}$ and V_{br} of the DTG MOSFET change as a function of t_d. Baliga's figure-of-merit is maximized for td=1.5 µm using this gadget. Fig.14, displays the dependence of $R_{on,sp}$ on V_{GS} for the DTG MOSFET. The higher the V_{GS}, the more ID there is, and hence the lower the $R_{on,sp}$. The $R_{on,sp}$is calculated to be 51 mm^2 at a V_{GS}, =10 V.

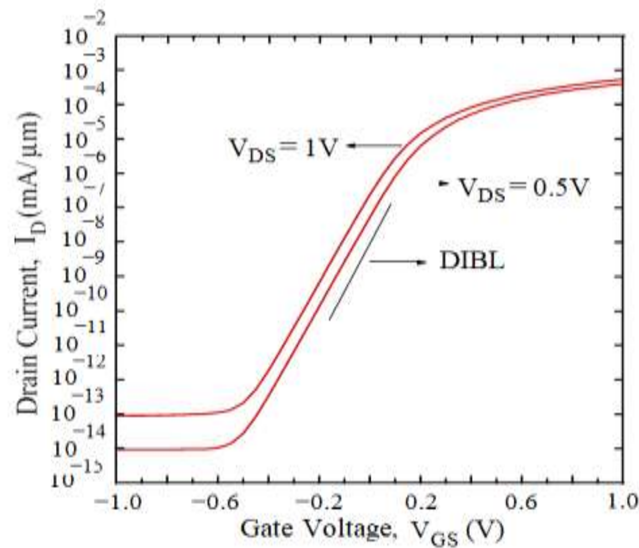

Figure 10: Typical low voltage MOSFET sub-threshold behavior.

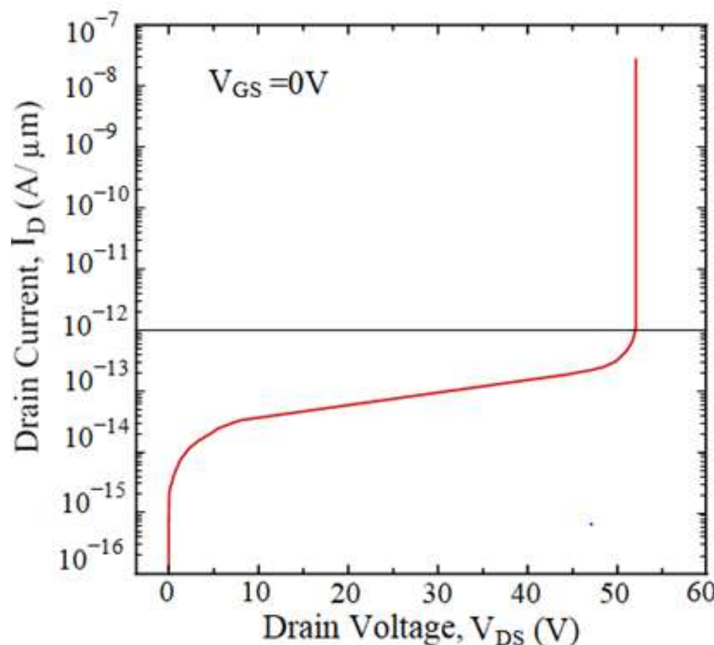

Figure 11: High voltage breakdown characteristics of a DTG MOSFET.

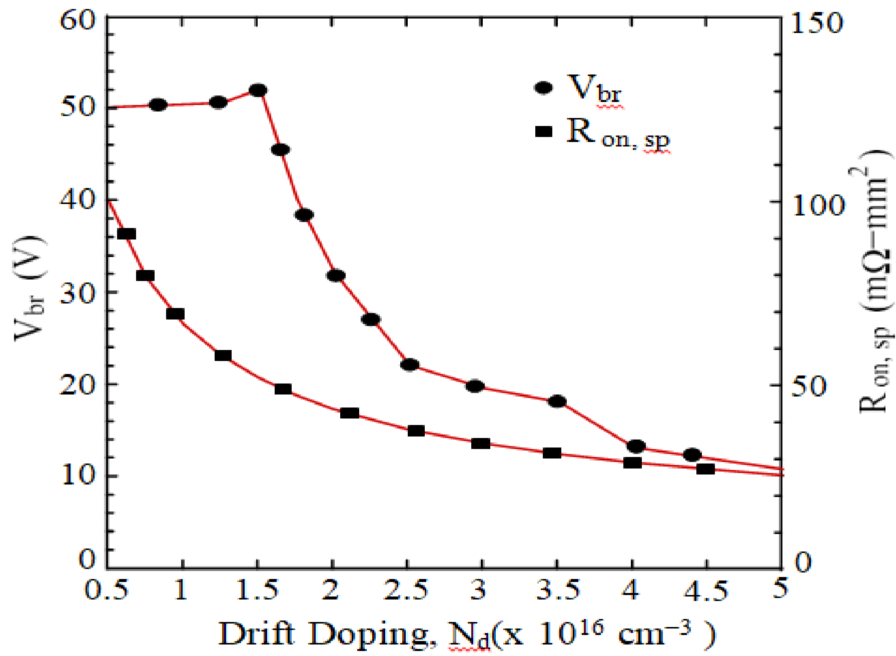

Figure 12: High-voltage DTG MOSFET V_{br} and $R_{on,sp}$vsNd.

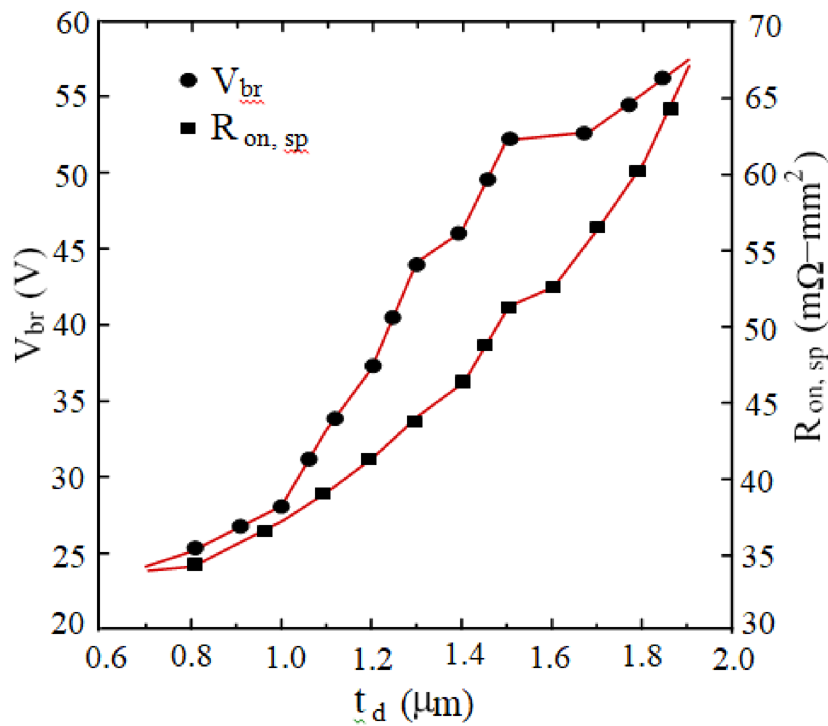

Figure 13: A plot of the high-voltage DTG MOSFET's V_{br} and Ron,spvs time-of-day.

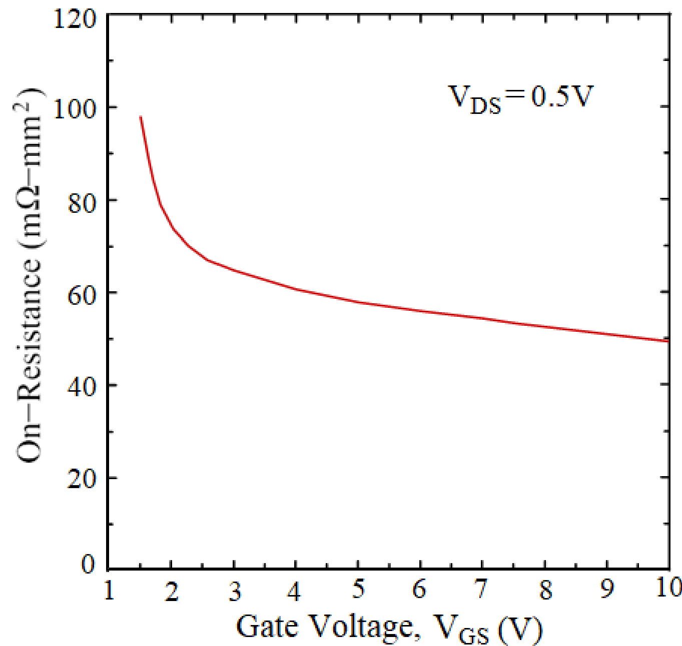

Figure 14: High voltage DTG MOSFET on resistance vs gate voltage.

4. CONCLUSION

In order to create smart power IC on InGaAs, it is suggested to combine high-voltage and low-voltage MOSFET architectures. Both devices' trench gates generate many p-base region channels, which increases ID and decreases Ron-sp. By increasing the precision with which the gate electrodes are positioned across the ID, ft and fmax of the proposed devices may be enhanced. Two-dimensional simulations performed in a device simulator are used to evaluate the performance differences between a high-voltage DTG MOS-FET or a low-voltage small-signal MOSFET. It is shown that the static and dynamic properties of both devices are satisfactory. The suggested idea may be utilized to create digital and analog high-frequency power integrated circuits.

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